APEX MICROTECHNOLOGY
PRECISION • POWER • ANALOG

VRE410

Precision Dual Voltage Reference

RoHS COMPLIANT

FEATURES

- ±10V Output, ± 1.6mV
- Temperature Drift: 1.0 ppm/°C
- Low Noise: $6\mu V_{P-P}$ (0.1-10 Hz)
- Tracking Error: 0.mV
- Excellent Line Regulation: 6ppm/V Typical
- Surface Mount Package

APPLICATIONS

The VRE410 is recommended for use as a reference for high precision D/A and A/D converters which require an external precision reference. The device is also ideal for calibrating scale factor on high resolution A/D converters. The VRE410 offers superior performance over monolithic references.

DESCRIPTION

The VRE410 is a low cost, high precision, ±10V reference. Available in a 14-pin SMT package, the device is ideal for new designs that need a high performance reference.

The device provides ultrastable ±10V output with ±1.6mV initial accuracy and a temperature coefficient of 1.0ppm/°C. This improvement in accuracy is made possible by a unique, patented multipoint laser compensation technique.

Another key feature of this reference is the 0.5mV tracking error between the positive and negative output voltages over the full operating temperature range. This is extremely important in high performance systems for reducing overall system errors.

SELECTION GUIDE

Model	Initial Error (mV)	Temp. Coeff. (ppm/°C)	Temp Range (°C)
VRE410AS	±1.6	1.0	0°C to +70°C
VRE410BS	±2.0	2.0	0°C to +70°C
VRE410JS	±1.6	1.0	-40°C to +85°C
VRE410LS	±2.2	2.2	-40°C to +85°C

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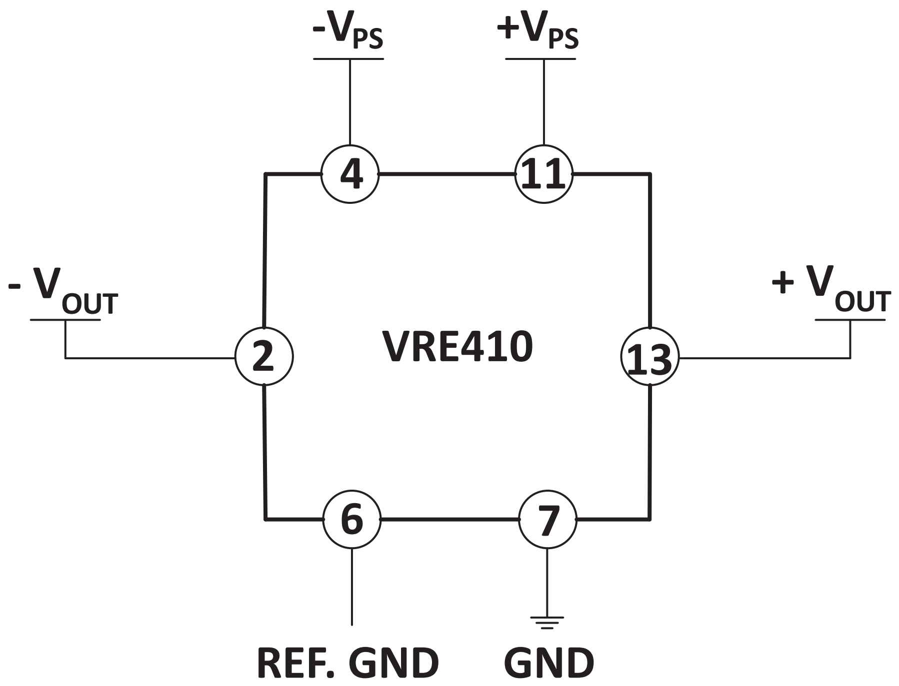
TYPICAL CONNECTION

Figure 1: Typical Connection



PIN DESCRIPTIONS

Pin Number	Name	Description
2	-OUT	-10V output.
4	$-V_{PS}$	The negative supply voltage connection.
6	REF_GND	Provided for accurate ground sensing. Internally connected to GND.
7	GND	Ground.
11	$+V_{PS}$	The positive supply voltage connection.
13	+OUT	+10V output.
All Others	NC	No connection.

SPECIFICATIONS

V_{PS} = +15V, T = +25°C, R_L = 10 kΩ unless otherwise noted.

ABSOLUTE MAX RATINGS

Parameter	A/J			B			L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply	±13.5	±15	±22	*	*	*	*	*	*	V
Operating Temperature (A,B)	0		+70	*		*	*		*	°C
Operating Temperature (J,L)	-40		+85	*		*	*		*	°C
Storage Temperature	-65		+150	*		*	*		*	°C
Short Circuit Protection	Continuous			*			*			
Soldering Temperature (10 sec max)			+260			*			*	°C

ELECTRICAL SPECIFICATIONS

Parameter	A/J			B			L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage		±10.0			*			*		V
Initial Error [1]			±1.60			±2.00			±2.20	mV
Warmup Drift		1			2			3		ppm
T_{MIN} - T_{MAX} [2]			1.0			2.0			2.2	ppm/°C
Tracking Error [3]		0.5			0.7			1.0		mV
Long-Term Stability		6			*			*		ppm/1000hrs
Noise (0.1 - 10Hz)		6			*			*		µVpp
Output Current	±10			*						mA
Line Regulation		3			*			*		ppm/V
Load Regulation		3			*			*		ppm/mA
Power Supply Current, +PS [4]		7			*			*		mA
Power Supply Current, -PS [4]		4			*			*		mA

1. The specified values are without external trim.
2. The temperature coefficient (TC) is determined by the box method using the following formula:

$$TC = \frac{V_{MAX} - V_{MIN}}{V_{NOMINAL} \times (T_{MAX} - T_{MIN})} \times 10^6$$

3. The tracking error is the deviation between the positive and negative output over the operating temp. range.
4. The specified values are unloaded.

Note: * Same as A/J Models

TYPICAL PERFORMANCE GRAPHS

Figure 2: V_{OUT} vs. Temperature (VRE410AS)

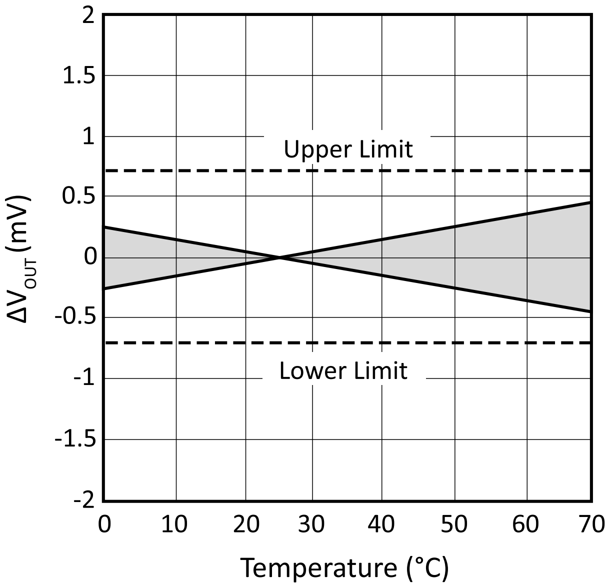


Figure 3: V_{OUT}vs. Temperature (VRE410BS)

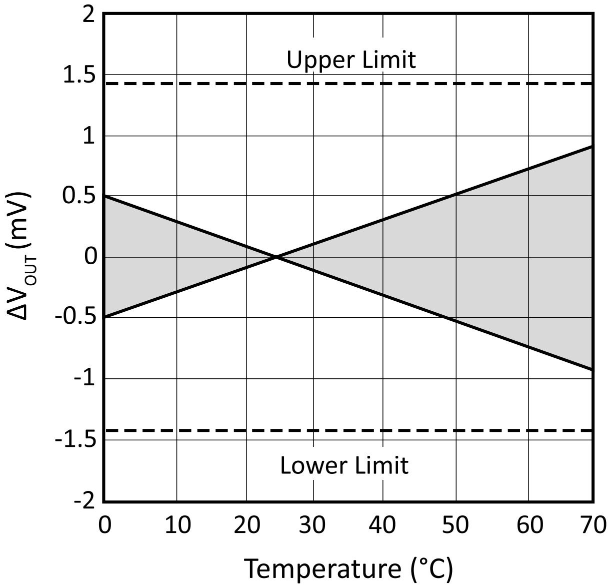


Figure 4: V_{OUT} vs. Temperature (VRE410JS)

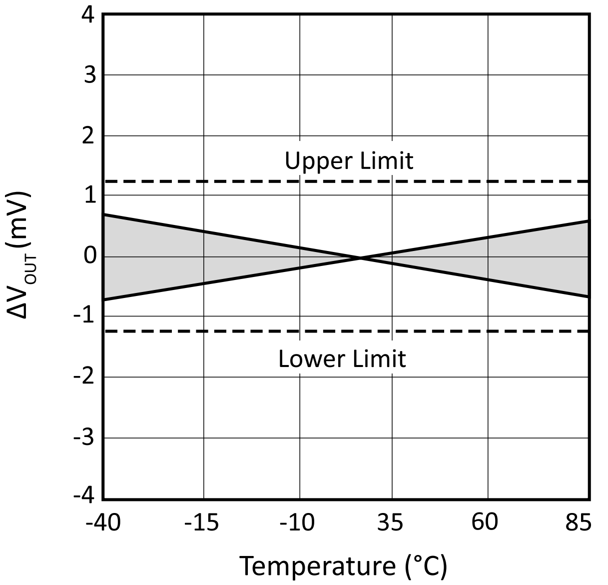
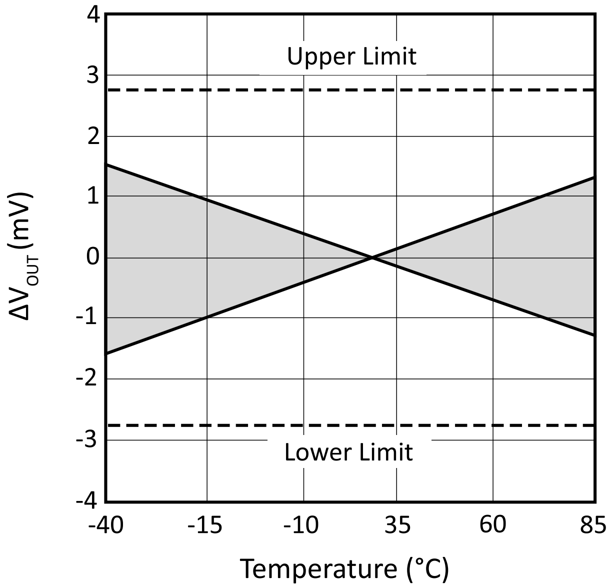


Figure 5: V_{OUT} vs. Temperature (VRE410LS)



POSITIVE OUTPUT (TYP)

Figure 6: Quiescent Current vs. Temperature

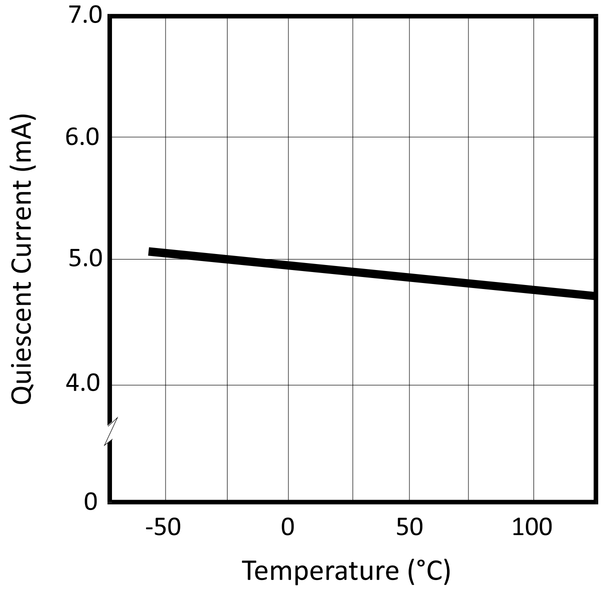


Figure 7: Junction Temp Rise vs. Output Current

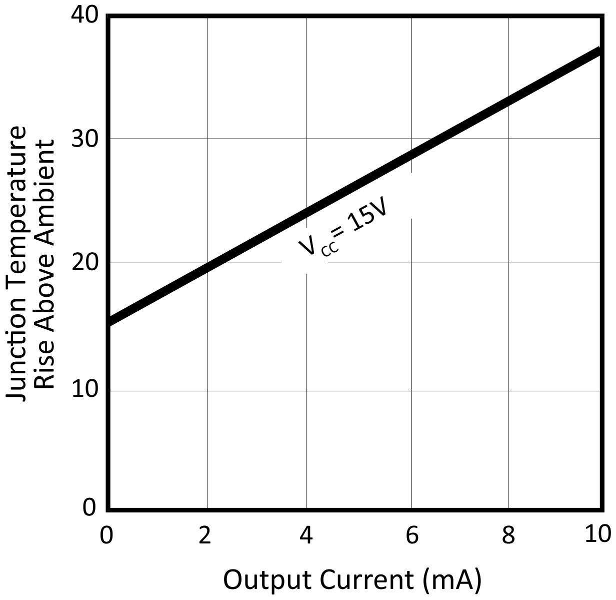
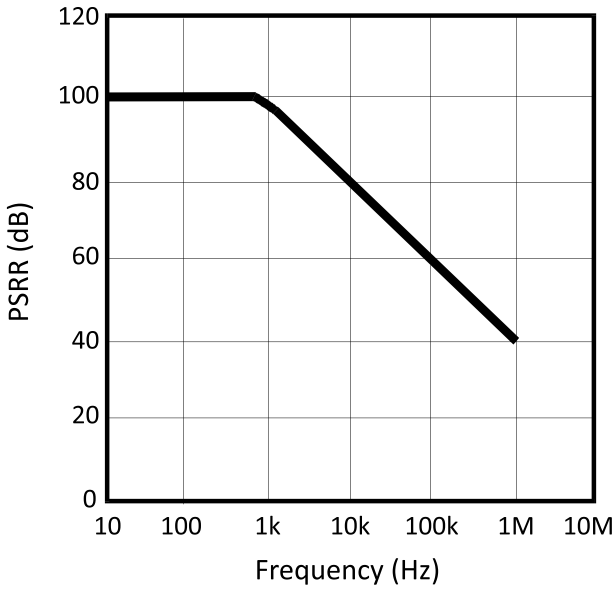


Figure 8: PSRR vs. Frequency



NEGATIVE OUTPUT (TYP)

Figure 9: Quiescent Current vs. Temperature

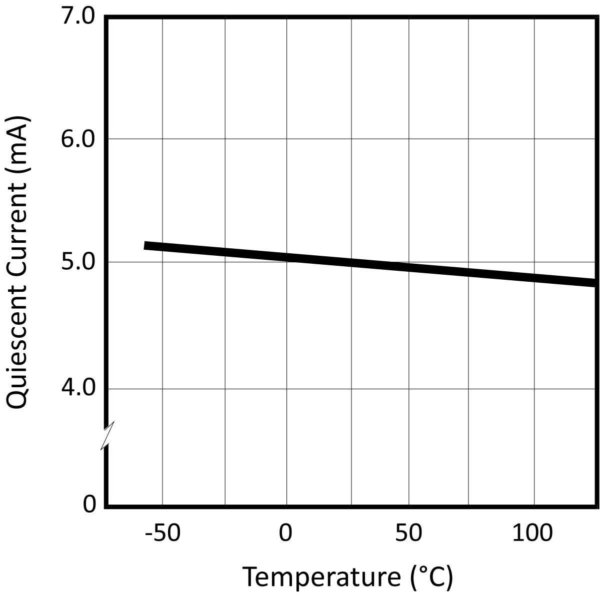


Figure 10: Junction Temp Rise vs. Output Current

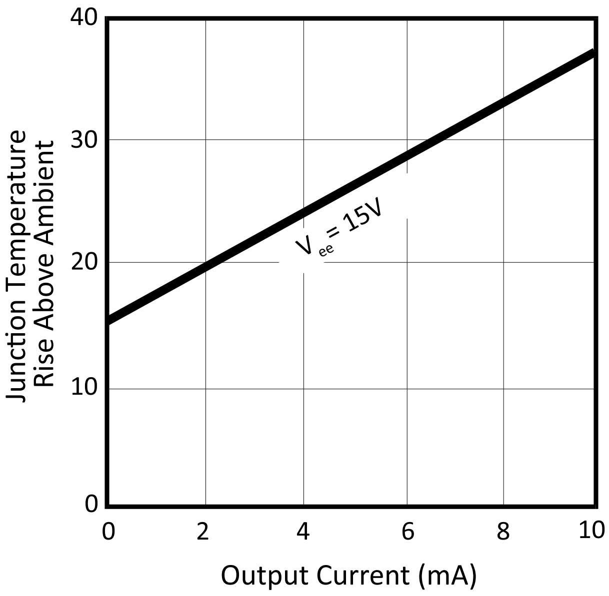
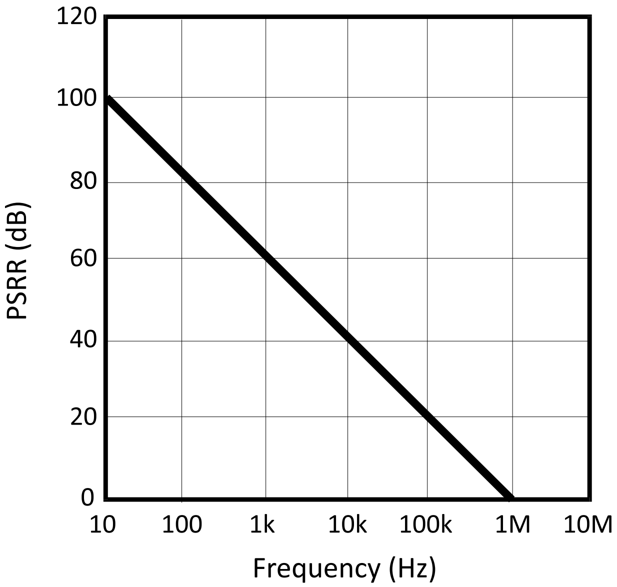
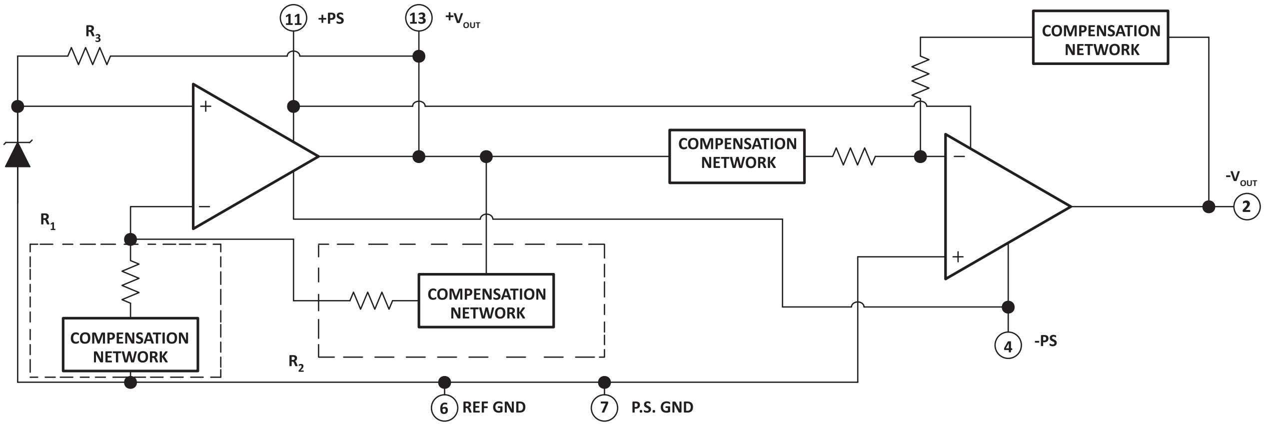


Figure 11: PSRR vs. Frequency



BLOCK DIAGRAM

Figure 12: Block Diagram



THEORY OF OPERATION

The following discussion refers to the block diagram in Figure 12. In operation, approximately 6.3V is applied to the noninverting input of the op amp. The voltage is amplified by the op amp to produce a 10V output. The gain is determined by the networks R1 and R2: G=1 + R2/R1. The 6.3V Zener diode is used because it is the most stable diode over time and temperature.

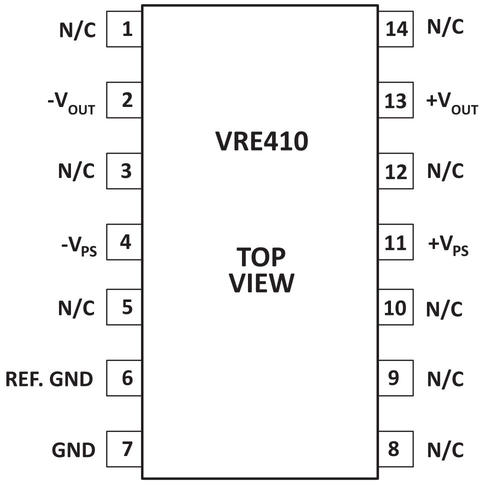
The Zener operating current is derived from the regulated output voltage through R3. This feedback arrangement provides a closely regulated Zener current. This current determines the slope of the references' voltage vs. temperature function. By trimming the Zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear this compensation technique is not well suited for wide temperature ranges.

A nonlinear compensation network of thermistors and resistors is used in the VRE series voltage references. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, a very stable voltage is produced over wide temperature ranges.

The VRE400 series voltage references have the ground terminal brought out on two pins (pin 6 and 7) which are connected together internally. This allows the user to achieve greater accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature, this voltage drop could be trimmed out. When the reference is plugged into a socket, this source of error can be as high as 20ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit, the error due to the contact resistance can be eliminated. If the unit is soldered into place the contact resistance is sufficiently small that it doesn't effect performance.

PIN CONFIGURATION

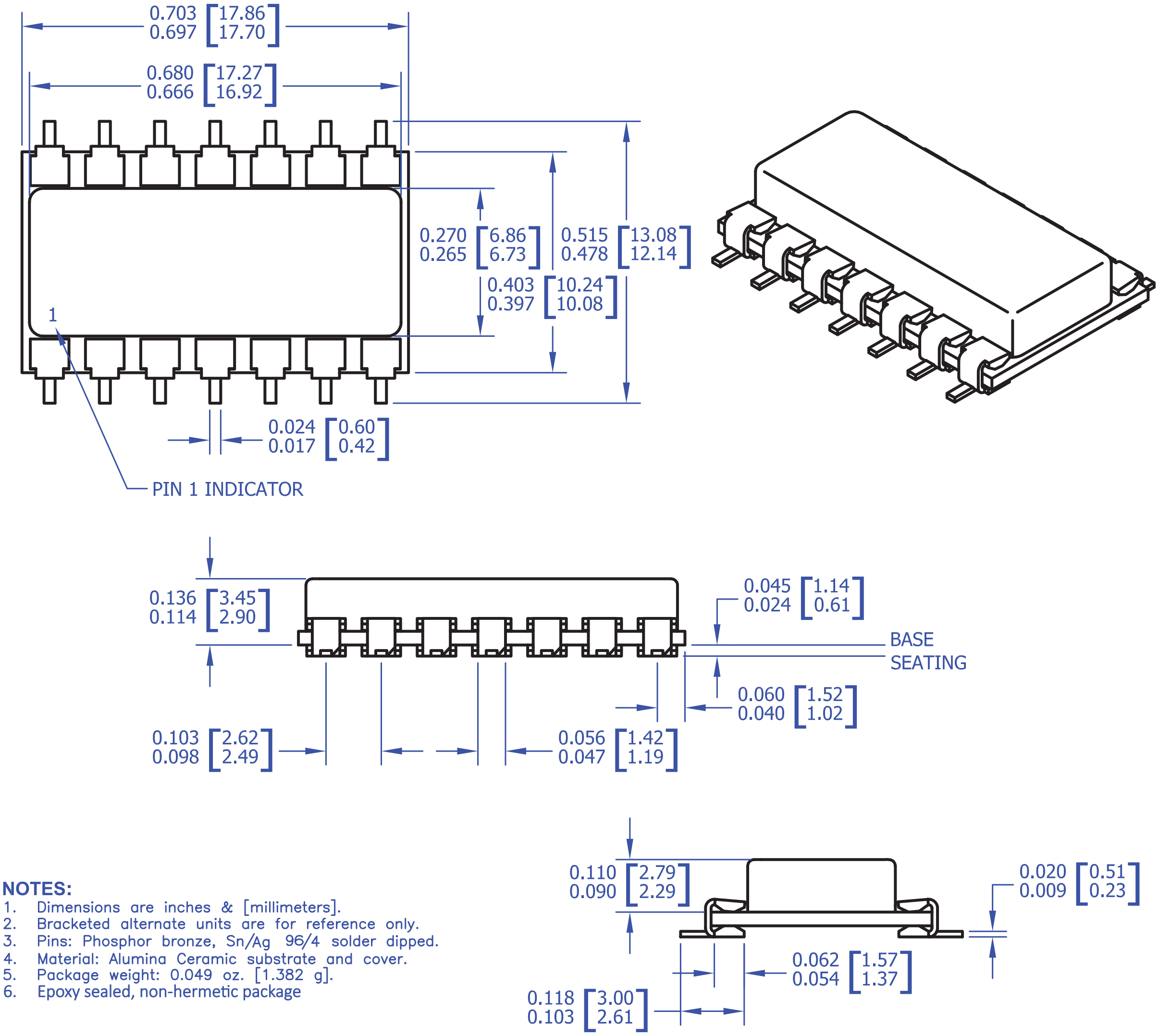
Figure 13: Pin Configuration



PACKAGE OPTIONS

Part Number	Apex Package Style	Description
VRE410AS	GE	14-pin SMT DIP
VRE410BS	GE	14-pin SMT DIP
VRE410JS	GE	14-pin SMT DIP
VRE410LS	GE	14-pin SMT DIP

PACKAGE STYLE GE



NOTES:

1. Dimensions are inches & [millimeters].
2. Bracketed alternate units are for reference only.
3. Pins: Phosphor bronze, Sn/Ag 96/4 solder dipped.
4. Material: Alumina Ceramic substrate and cover.
5. Package weight: 0.049 oz. [1.382 g].
6. Epoxy sealed, non-hermetic package

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